Subject Name: VLSI DESIGN

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Unit-I: Basic Electrical Properties

Important points / Definitions:

1.The four generations of Integration Circuits are
SSI (Small Scale Integration)
MSI (Medium Scale Integration)
LSI (Large Scale Integration)
VLSI (Very Large Scale Integration)

2.The advantages of IC are
Size is less
High Speed
Less Power Dissipation

3.The variety of Integrated Circuits?
More Specialized Circuits
Application Specific Integrated Circuits(ASICs)
Systems-On-Chips

4.The basic process for IC fabrication
Silicon wafer Preparation
Epitaxial Growth
Oxidation
Photolithography
Diffusion
Ion Implantation
Isolation technique
Metallization
Assembly processing & Packaging

5.The different types of oxidation are Dry & Wet Oxidation

6.The Enhancement mode transistor is the device that is normally cut-off with zero gate bias.

7.The Depletion mode Device is the Device that conduct with zero gate bias.

8.If a large Vds is applied this voltage with deplete the Inversion layer .This Voltage effectively pinches off the channel near the drain then the channel is said to be pinched –off

9.The different types of CMOS process
-p-well process, n-well process
-Silicon-On-Insulator Process
-Twin- tub Process

10.The steps involved in twin-tub process
Tub Formation
Thin-oxide Construction
Source & Drain Implantation
Contact cut definition
Metallization.

11.The basic processing steps involved in BiCMOS process
Additional masks defining P base region
N Collector area
Buried Sub collector (SCCD)
Processing steps in CMOS process

12.The advantages of CMOS Process are
Low power Dissipation
High Packing density
Bi directional capability
Low Input Impedance
Low delay Sensitivity to load.

13.To obtain the functional relationship among the terminal electrical variables of the device that is to be modeled.

14.Transistors with Channel length less than 3- 5 microns are termed as Short channel devices. With short channel devices the ratio between the lateral & vertical dimensions are reduced.

15.A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

16.A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

17. Why NMOS technology is preferred more than PMOS technology?
N- channel transistors has greater switching speed when compared tp PMOS transistors.

18.The different operating regions for an MOS transistor?
Cutoff region
Non- Saturated Region
Saturated Region

19.The different MOS layers?
n-diffusion
p-diffusion
Polysilicon
Metal

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Define threshold voltage of a MOS device.
2. What are pull-ups and write about the resistor pull-up and its usage.
3. Define gm of MOS transistor.
4. Draw transfer characteristics of CMOS inverter.
5. Define scaling and explain it.
6. What are the advantages of BiCMOS process compare with the CMOS.
7. What are the advantages of BiCMOS process compare with the CMOS.
8. List the fabrication procedures for IC Technologies.
9. Write about the Pass transistor.
10. Distinguish between Enhancement and Depletion mode transistor action in N-MOS.

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Draw the fabrication steps of CMOS transistor and explain its operation in detail.
2. Draw the fabrication steps of NMOS transistor and explain its operation in detail.
3. Explain the CMOS fabrication process in p-well using suitable diagrams.
4. Discuss the effect of threshold voltage on MOSFET current Equations.
5. Discuss the MOS transistor Characteristics in Depletion and enhancement modes.
6. Write about Alternative forms of pull-up and describe about the NMOS pull-ups.
7. Discuss the Basic Electrical Properties of MOS and BiCMOS Circuits.
8. Derive the expression for estimation of Pull-Up to Pull-Down ratio of an n-MOS inverter driven by another n-MOS inverter.
9. Write about BiCMOS fabrication in a n-well process with a diagram.
10. Distinguish between Bipolar and CMOS devices technologies in brief.
11. Mention about the BICMOS Inverters and alternative BICMOS Inverters.
12. Determine the pull-up to pull down ratio for NMOS inverter driven by another NMOS Inverter.

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1. Speed power product is measured as the product of [a]
a) gate switching delay and gate power dissipation
b) gate switching delay and gate power absorption
c) gate switching delay and net gate power
d) gate power dissipation and absorption

2. nMOS devices are formed in [c]
a) p-type substrate of high doping level
b) n-type substrate of low doping level
c) p-type substrate of moderate doping level
d) n-type substrate of high doping level

3. In MOS transistors, _____ is used for their gate [c]

a) metal
b) silicon-di-oxide
c) polysilicon
d) gallium

4. _____ impurities are added to the wafer of the crystal [b]
a) n impurities
b) p impurities
c) siicon
d) crystal

5. What kind of substrate is provided above the barrier to dopants? [a]
a) insulating
b) conducting
c) silicon
d) semi conducting

6. CMOS has [b]
a) high noise margin
b) high packing density
c) high power dissipation
d) high complexity

7.Oxidation process is carried out using [a]
a) hydrogen
b) low purity oxygen
c) sulphur
d) nitrogen

8.What are the advantages of BiCMOS? [d]
a) higher gain
b) high frequency characteristics
c) better noise characteristics
d) all of the mentioned

9. BiCMOS can be used in [b]
a) amplifyig circuit
b) driver circuits
c) divider circuit
d) multiplier circuit

10.Velocity can be given as [b]
a) μ / Vds
b) μ / Eds
c) μ x Eds
d) Eds / μ

11.gm is _____ to Ic [a]

a) directly proportional
b) inversely proportional
c) not dependent
d) exponentially proportional

12. The inverter has [a]
a) low input impedance
b) high input impedance
c) high output impedance
d) high input and output impedance

Unit-II VLSI Circuit Design Processes

Important points / Definitions:

1.Stick Diagram is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

2.The uses of Stick diagram are
It can be drawn much easier and faster than a complex layout.
These are especially important tools for layout built from large cells.

3.The various color coding used in stick diagram
Green – n-diffusion
Red- polysilicon
Blue –metal
Yellow- implant
Black-contact areas.

4.The Threshold voltage, is defined as V_T for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.

5.The threshold volatge V_T is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

6.The Channel-length modulation is defined as current between drain and source terminals is constant and independent of theapplied voltage over the terminals. This is not entirely correct. The effective length ofthe conductive channel is actually modulated by the applied V_{DS}, increasing V_{DS} causesthe depletion region at the drain junction to grow, reducing the length of the effectivechannel.

7.Latch up is a condition in which the parasitic components give rise to the

establishment of low resistance conducting paths between V_{DD} and V_{SS} with disastrous results. Careful control during fabrication is necessary to avoid this problem.

8.Rise time, τ_r is the time taken for a waveform to rise from 10% to 90% of its steady-state value.

9.Fall time, τ_f is the time taken for a waveform to fall from 90% to 10% of its steadystate value.

10.Delay time, τ_d is the time difference between input transition (50%) and the 50% output level. This is the time taken for a logic transition to pass from input to output.

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Explain difference between stick diagram and layout diagram.
2. Define delay and explain different time delays in gate level modeling.
3. Draw the VLSI Design Flow.
4. Draw the stick diagram for two inputs NOR gate.
5. What is switch logic?
6. What are the issues involved in driving large capacitive loads in VLSI circuits.
7. Explain about the contact cuts and approaches.
8. Represent the Stick diagram of a NMOS inverter.
9. Write about contacts and vias in layout design. [2]
10. Write about the 1.2 μm double metal single poly CMOS rules.

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Draw the flow chart of VLSI Design flow and explain the operation of each step in detail.
2. Draw the stick diagram for three input AND gate.
3. What is the purpose of design rule? What is the purpose of stick diagram? What are the different approaches for describing the design rule? Give three approaches for making contacts between poly silicon and discussion in NMOS circuit.
4. Discuss about the stick diagrams and their corresponding mask layout examples.
5. Draw the stick diagram of p-well CMOS inverter and explain the process.
6. Explain about the 2 μm CMOS Design rules and discuss with a layout example.
7. Draw and explain the layout for CMOS 2-input NAND gate.
8. Write about the stick diagrams and design a stick diagram for two input N-MOS NAND and NOR gates.
9. Distinguish between the Lambda-base rules and Double metal MOS process rules.
10. Draw the neat layout diagrams for NMOS shift register cell.

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1. Stick diagrams are those which convey layer information through [b]
a) thickness
b) color
c) shapes
d) layers

2. Which color is used for n-diffusion?[c]
a) red
b) blue
c) green
d) yellow

3.Which color is used for contact areas?[c]
a) red
b) brown
c) black
d) blue

4.Which color is used for polysilicon?[b]
a) brown
b) red
c) white
d) orange

5.Which color is used for buried contact?[d]
a) black
b) white
c) green
d) brown

6.The width of n-diffusion and p-diffusion layer should be[b]
a) 3λ
b) 2λ
c) λ
d) 4λ

7. What should be the spacing between two diffusion layers?[c]
a) 4λ
b) λ
c) 3λ
d) 2λ

8.What is the relationship between channel resistance and sheet resistance?[b]
a) R = Rs
b) R = Z*Rs
c) R = Z/Rs
d) R = Rs/Z

9. Which contribute to the wiring capacitance?[d]
a) fringing fields
b) interlayer capacitance
c) peripheral capacitance
d) all of the mentioned

10. Gate area is scaled by[c]
a) α
b) 1/α
c) $1/\alpha^2$
d) α^2

Unit III Gate Level Design

Important points / Definitions:

1.The inverter that uses a p-device pull-up or loads that has its gate permanently ground. An n-device pull-down or driver is driven with the input signal. This roughly equivalent to use of a depletion load is NMOS technology and is thus called 'Pseudo-NMOS

2.This logic looks into enhancing the speed of the pull up device by precharging the output node to Vdd. Hence we need to split the working of the device into precharge and evaluate stage for which we need a clock. Hence it is called as dynamic logic.

3.The sheet resistance is a measure of resistance of thin films that have a uniform thickness. It is commonly used to characterize materials made by semiconductor doping, metal deposition, resistive paste printing, and glass coating

4.Fan-In is defined as Number of inputs to a logic gate

5.Fan-Out (FO) is defined as Number of gate inputs which are driven by a particular gate output

6.Pass Transistor Logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Explain the importance of wiring capacitance of a MOS transistor.
2. Write about the clocked CMOS logic and its usage.
3. Explain about the Wiring capacitance and its need.
4. Mention the different forms of Time delays in gate level circuits.
5. Explain about Switch logic and its usage
6. Mention the different forms of Time delays in gate level circuits.
7. Explain about Switch logic and its usage.

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Draw and explain fan in and fan out characteristics of different CMOS design technologies.
2. Explain different wiring capacitance used in Gate level design with example7. What are the alternate gate circuits available? Explain any one of item with suitable sketch by taking NAND gate as an example.
3. Discuss about the logics implemented in gate level design and explain the switch logic
   implementation for a four way multiplexer.
4. Describe about the methods for driving large capacitive loads.
5. Describe about the choice of fan – in and fan – out selection in gate level design.
6. Describe the following:

a) Pseudo-nMOS Logic
b) Domino Logic.

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1.Switch logic is based on [c]
a) pass transistors
b) transmission gates
c) pass transistors and transmission gates
d) design rules

2.Switch logic is designed using [a]
a) complementary switches
b) silicon plates
c) conductors
d) resistors

3.As the number of inputs increases, the NAND gate delay [a]
a) increases
b) decreases
c) does not vary
d) exponentially decreases

4.In CMOS NAND gate, p transistors are connected in [b]

a) series
b) parallel
c) cascade
d) random

5.In CMOS NAND gate, p transistors are connected in [b]
a) series
b) parallel
c) cascade
d) random

6.BiCMOS is used for ____ fan-out [b]
a) less
b) more
c) no
d) very less

7.For a pseudo nMOS design the impedance of pull up and pull down ratio is [c]`
a) 4:1
b) 1:4
c) 3:1
d) 1:3

8.As the number of inputs increases, the NAND gate delay [a]
a) increases
b) decreases
c) does not vary
d) exponentially decreases

9.The CMOS inverter has _____ power dissipation [c]
a) low
b) more
c) no
d) very less

10.Features of switch logic approach [d]
a) occupies more area
b) no undesirable threshold voltage
c) low power dissipation
d) all of the mentioned

11.Pass transistor can be driven through _____ pass transistors [b]
a) one
b) no
c) more
d) two

Unit-IV: Data Path Subsystems

Important points / Definitions:

1.A data path is a collection of functional units, such as arithmetic logic units or multipliers that perform data processing operations, registers, and buses. Along with the control unit it composes the central processing unit (CPU).

2.The components of data path
• Register • Adder • Shifter • Multiplexer
3.A Shifter is most widely used for arithmetic operations. usually shifting is equivalent to multiplication by powers of two. Shifting is required during floating-point arithmetic. The shit register is simplest shifters that can shift by one position per clock cycle.

4.Barrel shifter produces n output bits and accepts 2n data bits , n control signals . The Barrel shifter shifts by transmitting a n-bits slice of the 2n data bits to the output.

5.An ALU is a Arithmetic Logic Unit that requires Arithmetic operations and Boolean operations. Basically arithmetic operations are addition and subtraction. one may either multiplex between an adder and a Boolean unit or merge the Boolean unit into the adder as in tha classic transistor-transistor logic

6.The magnitude of two binary numbers is compared by a magnitude comparator. Basically a comparator is build with an adder and an inverter.

7.Static random-access memory (SRAM) is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM), it does not need to be periodically refreshed, as SRAM uses bistable latching circuitry to store each bit.

8.Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Explain the difference between EPROM and EEPROM.
2. Draw 2-bit comparator.
3. Design a 2-bit Parity generator.
4. What is Booth's algorithm?
5. Mention about SRAM and its usage.
6. Describe about the Serial Access Memories.
7. Distinguish a synchronous and an asynchronous counters.
8. Write a note on Content Addressable Memory.

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Draw the basic circuit diagram of static RAM and explain its operation.
2. Draw the basic block diagram of 4-bit adder and explain its operation in detail. [5+5]
3. Explain the CMOS system design based on the I/O cells with suitable example.
4. Design a four bit parity generator using only XOR gates and draw the Schematic of it.
5. Draw the schematic and logic diagram for a single bit adder and explain its operation with truth table.
6. With neat circuit diagram, explain the operation of Barrel shifter. [5+5]
7. Explain about Serial access memories.
8. Design a shift register with the dynamic latch operated by a two-phase clock
9. Explain the working principle of Ripple carry adder using Transmission Gates
10. Explain about the Wallace tree multiplication and its design issues
11. Draw the circuit diagram of four transistor DRAM cell with storage nodes

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1.Flash memory is a non-volatile storage device in which data [c]
a) can be erased physically
b) can be erased magnetically
c) can be erased electrically
d) cannot be erased

2.NOR type flash allows _____ to be read or written independently [b]
a) one machine cycle
b) one machine word
c) one machine sentence
d) one bit

3.NAND type flash memories are used in [d]
a) memory cards
b) USB
c) solid state drivers
d) all of the mentioned

4.Which is comparatively slower device? [c]
a) ROM b) RAM
c) flash memory
d) SRAM

5.The transistors in NAND type flash are connected in [a]
a) series
b) parallel
c) cascade
d) randomly

6.Regularity is the ratio of [a]
a) total transistors in the chip to total transistors that must be designed in detail
b) total transistors that must be designed in detail to total transistors in chip
c) total transistors to total components
d) total charge storage components to charge dissipating components

7.Good design system has regularity in the range of [c]
a) 25-50
b) 50-75
c) 50-100
d) 25-50

8.The shifter must be connected to [d]
a) 2-shift data line
b) 2-shift control line
c) 4-shift data line
d) 4-shift control line

9.What is the sum and carry if the two bit number is 1 1 and the previous carry is 0? [b]
a) 0,0
b) 0,1
c) 1,0
d) 1,1

10.Which design is preferred in n-bit adder? [b]
a) many pass transistors in series
b) many pass transistors with suitable buffer
c) many pass transistors without suitable buffer
d) many pass transistors

11.In parallel Adder using ____ technology can be used for speed improvement [b]
a) CMOS
b) BiCMOS
c) nMOS
d) pMOS

12.Multiple output domino logic has [c]
a) two cell manchester carry chain
b) three cell manchester carry chain
c) four cell manchester carry chain
d) four cell manchester carry look ahead

Unit-V: Programmable Logic Devices & CMOS Testing

Important points / Definitions:

1.Functionality tests verify that the chip performs its intended function. These tests assert that all the gates in the chip, acting in concert, achieve a desired function. These tests are usually used early in the design cycle to verify the functionality of the circuit.

2.Manufacturing tests verify that every gate and register in the chip functions correctly. These tests are used after the chip is manufactured to verify that the silicon is intact.

3.The observability of a particular internal circuit node is the degree to which one can observe that node at the outputs of an integrated circuit.

4.The controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state.

5.The total number of nodes that, when set to 1 or 0, do result in the detection of the fault, divided by the total number of nodes in the circuit, is called the percentage-fault coverage.

6.Fault grading consists of two steps. First, the node to be faulted is selected. A simulation is run with no faults inserted, and the results of this simulation are saved. Each node or line to be faulted is set to 0 and then 1 and the test vector setis applied. If and when a discrepancy is detected between the faulted circuit response and the good circuit response, the fault is said to be detected and the simulation is stopped

.

7.An approach to fault analysis is known as fault sampling. This is used in circuits where it is impossible to fault every node in the circuit. Nodes are randomly selected and faulted. The resulting fault detection rate may be statistically inferred from the number of faults that are detected in the fault set and the size of the set. The randomly selected faults are unbiased. It will determine whether the fault coverage exceeds a desired level.

8.Signature analysis can be merged with the scan technique to create a structure known as BILBO- for Built In Logic Block Observation.

9.A popular method of testing for bridging faults is called IDDQ or current- supply monitoring. This relies on the fact that when a complementary CMOS logic gate is not switching, it draws no DC current. When a bridging

fault occurs, for some combination of input conditions a measurable DC I_{DD} will flow.

10.Th applications of chip level test techniques?
a. Regular logicarrays b. Memoriesc. Randomlogic

11The increasing complexity of boards and the movement to technologies like multichip modules and surface-mount technologies resulted in system designers agreeing on a unified scan-based methodology for testing chips at the board. This is called boundary scan.

12.The Test Access Port (TAP) is a definition of the interface that needs to be included in an IC to make it capable of being included in a boundary-scan architecture.

13.The test-data registers are used to set the inputs of modules to be tested, and to collect the results of running tests.

14.The boundary scan register is a special case of a data register. It allows circuit-board interconnections to be tested, external components tested, and the state of chip digital I/Os to be sample

15.In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

16.A cell-based ASIC (CBIC) USES PREDESIGNED LOGIC CELLS KNOWN AS STANDARD CELLS. The standard cell areas also called fle4xible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

17. A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Explain difference between PLA and PAL. [2]
2. Define controllability and observability with respect to testing. [3]
3. Write the Comparison between FPGA and CPLD. [2]
4. What type of faults can be reduced by improving layout design? [3]
5. Explain about the principle of Built in Self Test. [2]
6. Explain about test Principles used for testing. [3]
7. What is the need for testing of IC? [2]
8. What are the different chip-level Test Techniques

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Why the chip testing is needed? At what levels testing a chip can occur?
2. Explain the detailed Architecture of CPLD and its Implementations.
3. Write a short note on the following:
   a)CMOS Testing
   b)Strategies for testing
4. What is the drawback of serial scan? How to overcome this?
5. Briefly Explain different parameters influencing low power design in detail.
6. What is sequential fault grading? Explain how it is analyzed.
7. Explain Architecture of FPGA in detail.
8. What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits?
9. Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram.
10. Explain the detailed logic configurable Block Architecture of FPGA.
11. Explain the following in detail.
    a)Chip level Test Techniques
    b)Testability and practices.

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1.Electromigration is a [c]
a) processing fault
b) material defects
c) time dependent failure
d) packaging fault

2.Which relation is correct? [b]
a) failure – error – fault
b) fault – error – failure
c) error – fault – failure
d) error – failure – fault

3.For a circuit with k lines, ____ single stuckat fault is possible [b]
a) k
b) 2k
c) k/2

d) k

4. For a n signal lines circuit, _____ bridging faults are possible [c]
a) n
b) 2n
c) n
d) n/2

5. IDDQ fault occurs when there is [b]
a) increased voltage
b) increased quiescent current
c) increased power supply
d) increased discharge

6. Which fault causes output floating? [a]
a) stuck-open
b) stuck-at
c) stuck-on
d) IDDQ

7. The number of paths _____ with number of gates [a]
a) increases exponentially
b) decreases exponentially
c) remains the same
d) increases rapidly

8. Faults which produce same faulty behaviour are known as [b]
a) similar faults
b) equivalent faults
c) correlative faults
d) ambigious faults

9. Stuck-at fault is an example of _____ fault model [b]
a) transient
b) permanent
c) intermittent
d) simple

10. The signature analysis method can be represented mathematically as [b]
a) R(x) = P(x) * C(x)
b) R(x) = P(x) / C(x)
c) R(x) = C(x) / P(x)
d) R(x) = C(x) * P(x)